# DATA SHEET

## SA5214

## Postamplifier with link status indicator

Product specification

Replaces datasheet NE/SA5214 of 1995 Apr 26

IC19 Data Handbook

1998 Oct 07

**Philips**
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# Postamplifier with link status indicator

# SA5214

## DESCRIPTION

The SA5214 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The SA5214 can be DC coupled with the previous transimpedance stage using SA5210, SA5211 or SA5212 transimpedance amplifiers. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide noise filtering, adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The SA5214 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The SA5214 is designed as a companion to the SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the post-amplifier inputs. The SA5212/5214 or SA5211/5214 combinations convert nanoamps of photodetector current into standard digital TTL levels.

## APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Metropolitan Area Networks (MAN)
- Synchronous Optical Networks (SONET)
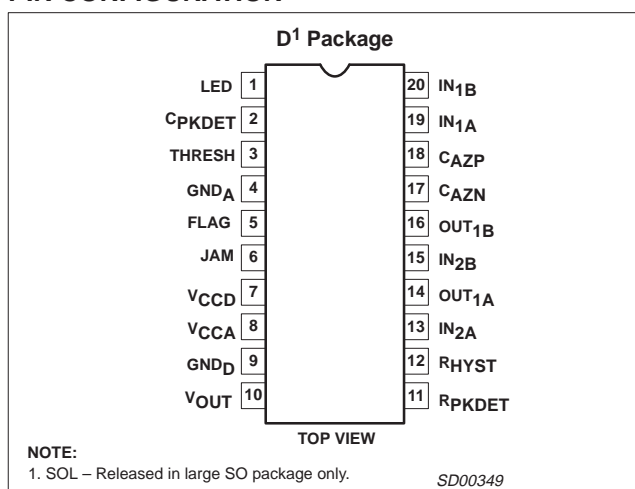- RF limiter

## PIN CONFIGURATION



**D[1] Package**

| | | | |
|---|---|---|---|
| LED | 1 | 20 | IN$_{1B}$ |
| C$_{PKDET}$ | 2 | 19 | IN$_{1A}$ |
| THRESH | 3 | 18 | C$_{AZP}$ |
| GND$_A$ | 4 | 17 | C$_{AZN}$ |
| FLAG | 5 | 16 | OUT$_{1B}$ |
| JAM | 6 | 15 | IN$_{2B}$ |
| V$_{CCD}$ | 7 | 14 | OUT$_{1A}$ |
| V$_{CCA}$ | 8 | 13 | IN$_{2A}$ |
| GND$_D$ | 9 | 12 | R$_{HYST}$ |
| V$_{OUT}$ | 10 | 11 | R$_{PKDET}$ |

**TOP VIEW**

**NOTE:**
1. SOL – Released in large SO package only.

SD00349

**Figure 1. Pin Configuration**

## FEATURES

- Postamp for the SA5211/5212 preamplifier family
- Wideband operation: typical 75MHz (100MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Low signal output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG # |
|---|---|---|---|
| 20-Pin Plastic Small Outline Large (SOL) Package | -40°C to +85°C | SA5214D | SOT163-1 |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| V$_{CCA}$ | Power supply | +6 | V |
| V$_{CCD}$ | Power supply | +6 | V |
| T$_A$ | Operating ambient temperature range | -40 to +85 | °C |
| T$_J$ | Operating junction temperature range | -55 to +150 | °C |
| T$_{STG}$ | Storage temperature range | -65 to +150 | °C |
| P$_D$ | Power dissipation | 300 | mW |
| V$_{IJ}$ | Jam input voltage | -0.5 to 5.5 | V |

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## PIN DESCRIPTIONS

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | LED | Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON. |
| 2 | $C_{PKDET}$ | Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor. |
| 3 | THRESH | Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector. |
| 4 | $GND_A$ | Device analog ground pin. |
| 5 | FLAG | Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two. |
| 6 | JAM | Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible. |
| 7 | $V_{CCD}$ | Power supply pin for the digital portion of the chip. |
| 8 | $V_{CCA}$ | Power supply pin for the analog portion of the chip. |
| 9 | $GND_D$ | Device digital ground pin. |
| 10 | $V_{OUT}$ | TTL output pin with a fanout of five. |
| 11 | $R_{PKDET}$ | Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, $C_{PKDET}$. |
| 12 | $R_{HYST}$ | Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector. |
| 13 | $IN_{2A}$ | Non-inverting input to amplifier A2. |
| 14 | $OUT_{1A}$ | Non-inverting output of amplifier A1. |
| 15 | $IN_{2B}$ | Inverting input to amplifier A2. |
| 16 | $OUT_{1B}$ | Inverting output of amplifier A1. |
| 17 | $C_{AZN}$ | Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1. |
| 18 | $C_{AZP}$ | Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1. |
| 19 | $IN_{1A}$ | Non-inverting input of the preamp A1. |
| 20 | $IN_{1B}$ | Inverting input of the preamp A1. |

## BLOCK DIAGRAM
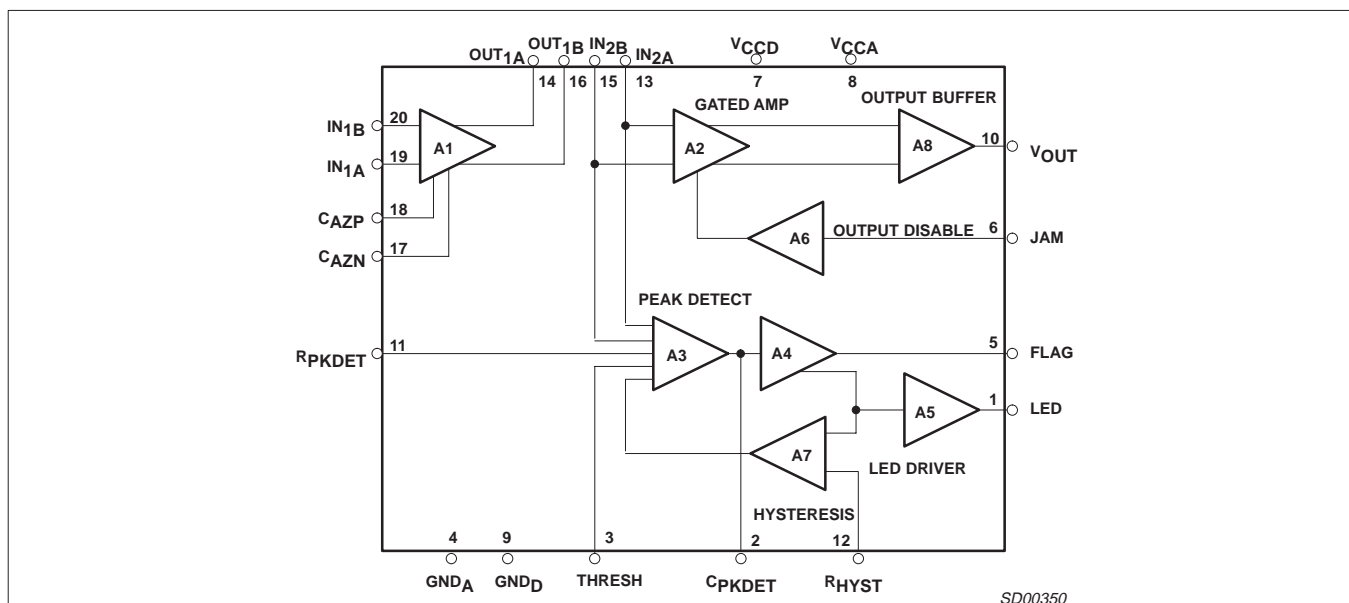


**Figure 2. Block Diagram**

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### RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CCA}$ | Supply voltage | 4.75 to 5.25 | V |
| $V_{CCD}$ | Power supply | 4.75 to 5.25 | V |
| $T_A$ | Ambient temperature range | -40 to +85 | °C |
| $T_J$ | Operating junction temperature range | -40 to +110 | °C |
| $P_D$ | Power dissipation | 250 | mW |

### DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA}=V_{CCD}=+5.0V$ unless otherwise specified. Typical data applies at $V_{CCA}=V_{CCD}=+5.0V$ and $T_A=25°C$.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{CCA}$ | Analog supply current | | | 30 | 41.2 | mA |
| $I_{CCD}$ | Digital supply current (TTL, Flag, LED) | | | 10 | 13.5 | mA |
| $V_{I1}$ | A1 input bias voltage (+/- inputs) | | 3.08 | 3.4 | 3.70 | V |
| $V_{O1}$ | A1 output bias voltage (+/- outputs) | | 3.10 | 3.8 | 4.50 | V |
| $A_{V1}$ | A1 DC gain (without Auto-Zero) | | | 30 | | dB |
| $A1_{PSRR}$ | A1 PSRR ($v_{CCA}$, $V_{CCD}$) | $V_{CCA}=V_{CCD}=4.75$ to 5.25V | | 60 | | dB |
| $A1_{CMRR}$ | A1 CMRR | $\Delta V_{CM}=200mV$ | | 60 | | dB |
| $V_{I2}$ | A2 input bias voltage (+/- inputs) | | 3.56 | 3.7 | 3.86 | V |
| $V_{OH}$ | High-level TTL output voltage | $I_{OH}=-200\mu A$ | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level TTL output voltage | $I_{OL}=8mA$ | | 0.3 | 0.4 | V |
| $I_{OH}$ | High-level TTL output current | $V_{OUT}=2.4V$ | | -40 | -24.4 | mA |
| $I_{OL}$ | Low-level TTL output current | $V_{OUT}=0.4V$ | 7.0 | 30 | | mA |
| $I_{OS}$ | Short-circuit TTL output current | $V_{OUT}=0.0V$ | | -95 | | mA |
| $V_{THRESH}$ | Threshold bias voltage | Pin 3 Open | | 0.75 | | V |
| $V_{RPKDET}$ | RPKDET | Pin 11 Open | | 0.72 | | V |
| $V_{RHYST}$ | RHYST bias voltage | Pin 12 Open | | 0.72 | | V |
| $V_{IHJ}$ | High-level jam input voltage | | 2.0 | | | V |
| $V_{ILJ}$ | Low-level jam input voltage | | | | 0.8 | V |
| $I_{IHJ}$ | High-level jam input current | $V_{IJ}=2.7V$ | | | 30 | $\mu A$ |
| $I_{ILJ}$ | Low-level jam input current | $V_{IJ}=0.4V$ | -485 | -240 | | $\mu A$ |
| $V_{OHF}$ | High-level flag output voltage | $I_{OH}=-80\mu A$ | 2.4 | 3.8 | | V |
| $V_{OLF}$ | Low-level flag output voltage | $I_{OL}=3.2mA$ | | 0.33 | 0.4 | V |
| $I_{OHF}$ | High-level flag output current | $V_{OUT}=2.4V$ | | -18 | -5 | mA |
| $I_{OLF}$ | Low-level flag output current | $V_{OUT}=0.4V$ | 3.25 | 10 | | mA |
| $I_{SCF}$ | Short-circuit flag output current | $V_{OUT}=0.0V$ | -61 | -40 | -26 | mA |
| $I_{LEDH}$ | LED ON maximum sink current | $V_{LED}=3.0V$ | 8 | 22 | 80 | mA |

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## AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
| --- | --- | --- | --- | --- | --- | --- |
| | | | Min | Typ | Max | |
| $f_{OP}$ | Maximum operating frequency | Test circuit | 60 | 75 | | MHz |
| $BW_{A1}$ | Small signal bandwidth (differential $OUT_1/IN_1$) | Test circuit | | 75 | | MHz |
| $V_{INH}$ | Maximum Functional A1 input signal (single ended) | Test Circuit | | 1.6 | | $V_{P-P}$ |
| $V_{INL}$ | Minimum Functional A1 input signal (single ended) | Test CIrcuit[1] | | 12 | | $mV_{P-P}$ |
| $R_{IN1}$ | Input resistance (differential at $IN_1$) | | | 1200 | | $\Omega$ |
| $C_{IN1}$ | Input capacitance (differential at $IN_1$) | | | 2 | | pF |
| $R_{IN2}$ | Input resistance (differential at $IN_2$) | | | 1200 | | $\Omega$ |
| $C_{IN2}$ | Input capacitance (differential at $IN_2$) | | | 2 | | pF |
| $R_{OUT1}$ | Output resistance (differential at $OUT_1$) | | | 25 | | $\Omega$ |
| $C_{OUT1}$ | Output capacitance (differential at $OUT_1$) | | | 2 | | pF |
| $V_{HYS}$ | Hysteresis voltage | Test circuit | | 3 | | $mV_{P-P}$ |
| $V_{THR}$ | Threshold voltage range (FLAG ON) | Test circuit, @ 50MHz $R_{RHYST}$=5k $R_{THRESH}$=47k | | 12 | | $mV_{P-P}$ |
| $t_{TLH}$ | TTL Output Rise Time 20% to 80% | Test Circuit | | 1.3 | | ns |
| $t_{THL}$ | TTL Output Fall Time 80% to 20% | Test Circuit | | 1.2 | | ns |
| $t_{RFD}$ | $t_{TLH}/t_{THL}$ mismatch | | | 0.1 | | ns |
| $t_{PWD}$ | Pulse width distortion of output | $50mV_{P-P}$, 1010. . .input $Distortion= \dfrac{T_H-T_L}{T_H+T_L} 10^2$ 2.5 | | | | 2.5 | % |

**NOTES:**
1. The SA5214 is capable of detecting a much lower input level. Operation under $12mV_{P-P}$ cannot be guaranteed by present day automatic testers.

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**Figure 3. AC Test Circuit**

## TYPICAL PERFORMANCE CHARACTERISTICS



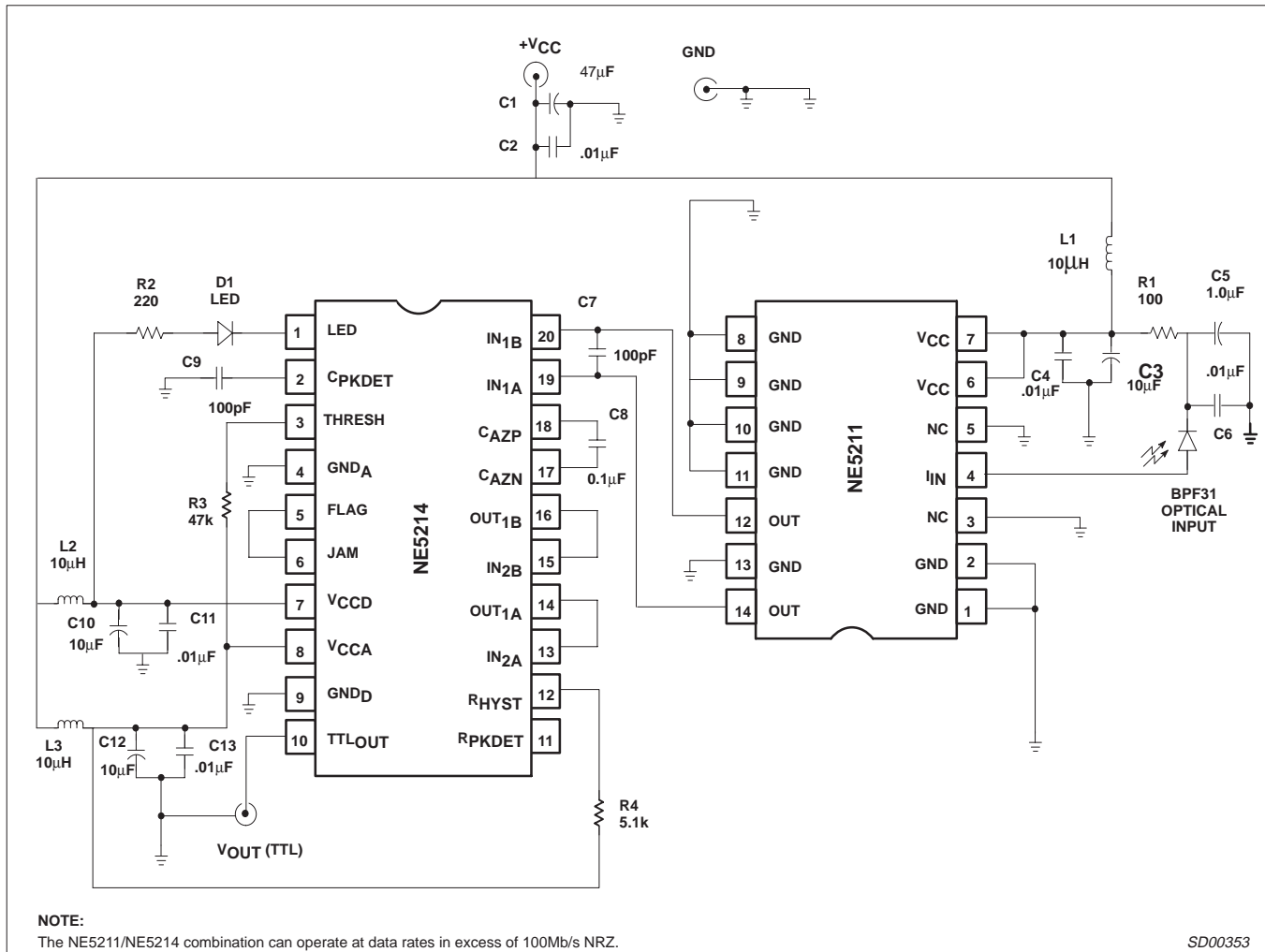**Figure 4. Typical Performance Characteristics**

**Figure 5.  A 50Mb/s Fiber Optic Receiver**

## THEORY OF OPERATION AND APPLICATION INFORMATION

The SA5214 postamplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

The SA5214 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the SA5214 to be directly connected to a transimpedance amplifier such as the SA5210, SA5211, or SA5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the SA5214 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the SA5214 Theory of

Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et al.

A typical application of the SA5214 postamplifier is depicted in Figure 5. The system uses the SA5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to AB 1432.

### Die Sales Disclaimer

Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

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All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

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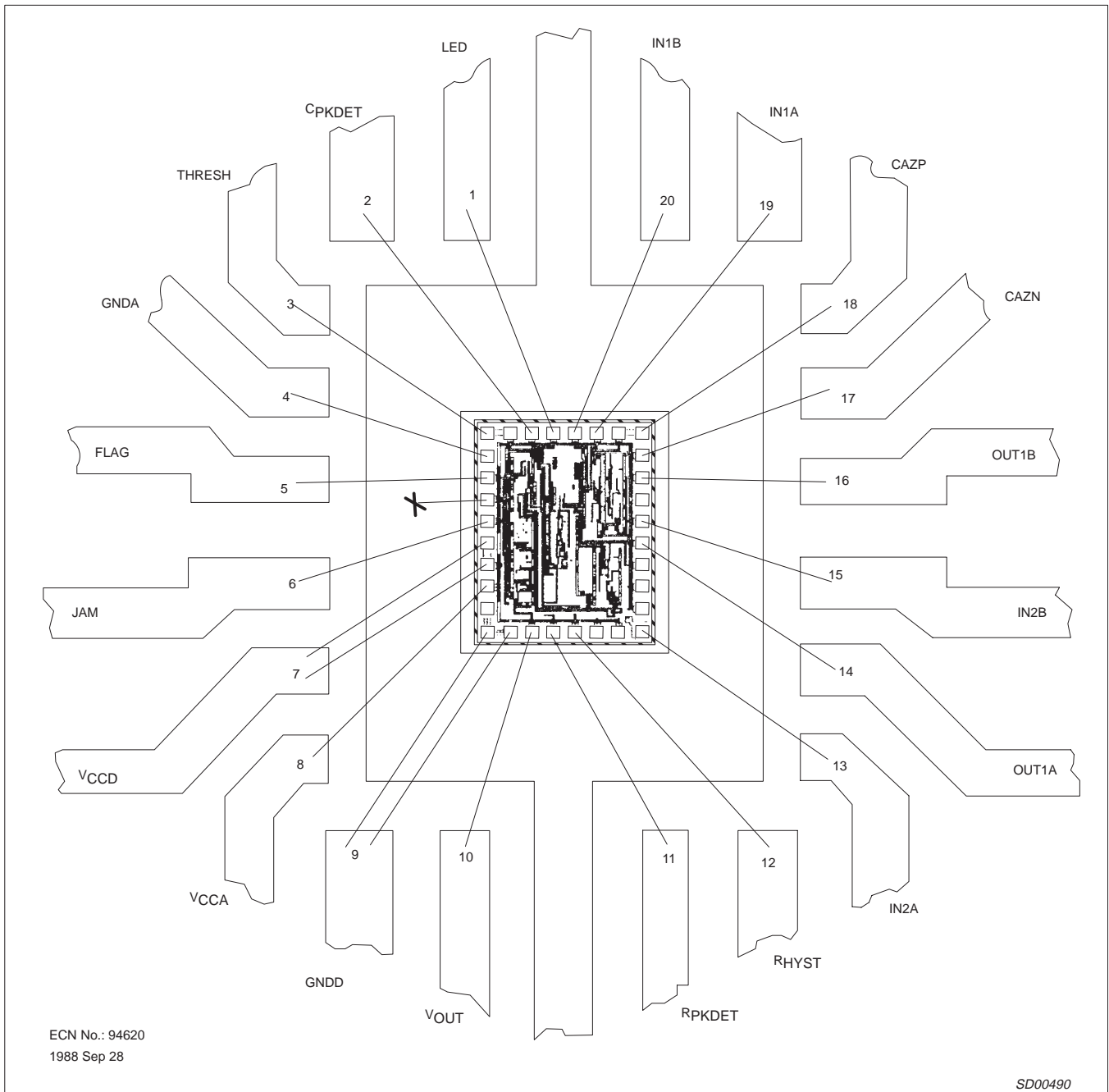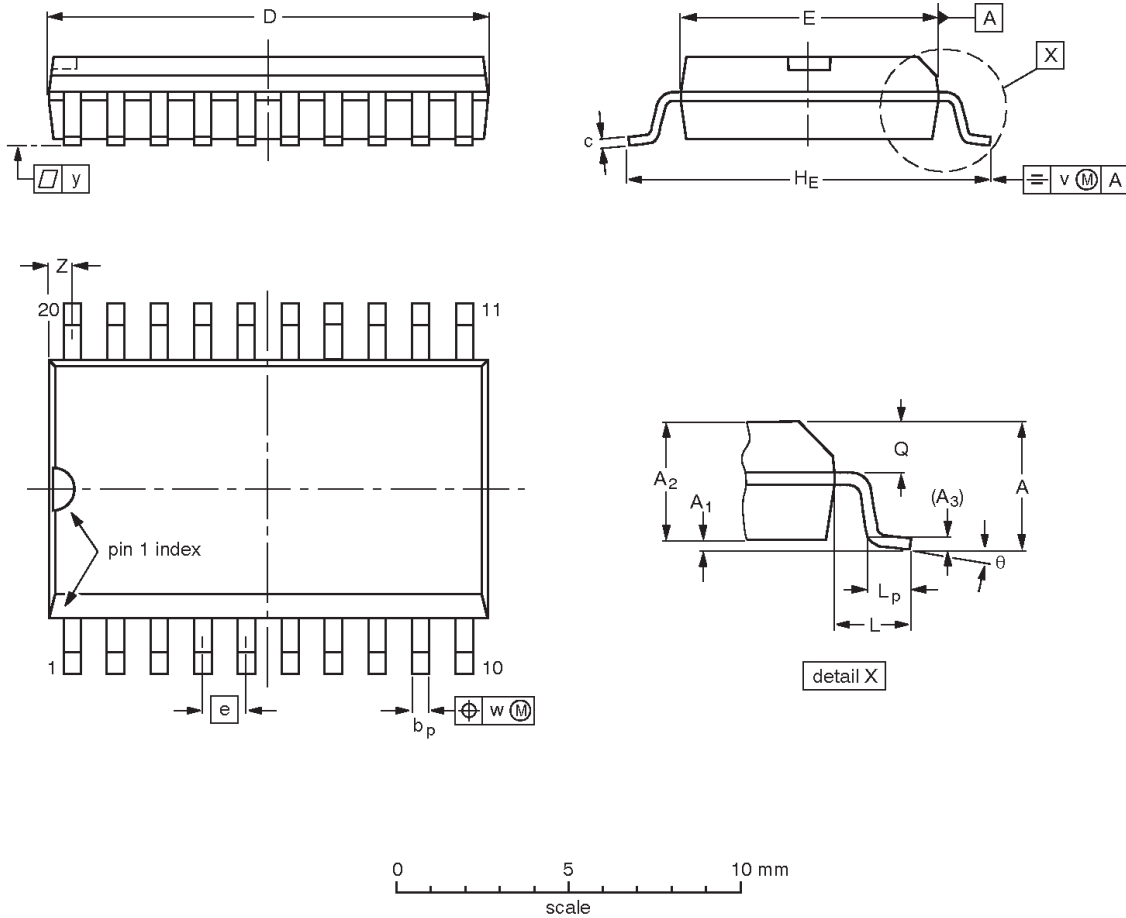


ECN No.: 94620
1988 Sep 28

SD00490

**Figure 6.  SA5214 Bonding Diagram**

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**SO20:   plastic small outline package; 20 leads; body width 7.5 mm**                                    **SOT163-1**



pin 1 index

detail X

0          5          10 mm

scale

**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D(1) | E(1) | e | HₑE | L | Lₚ | Q | v | w | y | Z(1) | θ |
|------|--------|----|----|----|----|----|------|------|---|-----|---|----|----|----|----|----|----|----|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 13.0 12.6 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.51 0.49 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|---|---|---|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | ~~95-01-24~~ 97-05-22 |

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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[1]   Please consult the most recently issued datasheet before initiating or completing a design.

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